UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/066,100	01/30/2002	Igor Guskov	01339.0008.NPUS00	6027

7590 04/28/2004

Robert C. Laurenson
HOWREY SIMON ARNOLD & WHITE, LLP
301 Ravenswood Avenue
Menlo Park, CA 94025

EXAMINER	
NGUYEN, KIMBINH T	
ART UNIT	**PAPER NUMBER**
2671	8

DATE MAILED: 04/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/066,100	GUSKOV ET AL.	
	Examiner	Art Unit	
	Kimbinh T. Nguyen	2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *43-48* is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to amendment filed 02/12/04.

2. Claims 1-48 are pending in the application.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-8, 11, 12, 15, 16, 22-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Loop (5,602,979) in view of Assa et al. (6,313,837).

Claim 1, Loop discloses forming a base mesh (input mesh M0; col. 6, lines 5-6); forming one or more higher level meshes (new meshes M1 and M2; col. 6, lines 8-11) from the base mesh through regular refinement operations in combination with irregular operation (isolating irregularities and constraining geometry or constrained refinement operation; col. 6, lines 5-7); Loop does not teach the hybrid mesh representation comprising the base mesh in combination with one or more higher level meshes; however, Assa et al. teaches a hierarchical surface representation is an architecture of a hybrid-grid mesh (col. 11, lines 54-67), because the quadtree hierarchy provides a multiresolution hierarchy which has an ancestor (base level of base mesh) and four children (higher levels), the hybrid grid-mesh representation supports general

topological and geometrical editing, the hybrid architecture maintains the flexibility to provide the irregular refinement of a grid (col. 12, lines 1-52). It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the hybrid representation as taught by Assa into the method of generating smooth low degree polynomial surfaces over irregular meshes of Loop's teaching for producing the hybrid mesh, because the hybrid architecture maintains the flexibility to provide the irregular refinement of a grid which would easily model multi-valued surfaces and surfaces which are rapidly changing in one area and flat in another (efficient classification and coherency algorithm; col. 12, lines 27-30).

Claims 2 -6, Loop discloses the base mesh (M0) is a regular mesh (col. 9, lines 27-28); the base mesh is an irregular mesh (col. 6, lines 6-8); the mesh comprises tessellated polygons (col. 8, lines 61-63); the polygons are quads (quad nets; col. 6, lines 13-14), are triangles (Bezier triangle; col. 6, line 15), **Claim 7**, Loop does not teach the polygons are hexagon; however, Loop teaches polynomial spline surface is constructed of degree 3 as opposed to 6 for bicubic surfaces (col. 5, lines 35-37). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the bicubic surfaces as taught by Loop for proving hexagon polygon, because using polynomial for ray tracing, the shape would render faster and more robust and generate aesthetically pleasing shapes (col. 14, lines 4-43).

Claims 11 and 12 Loop teaches polygons (meshes) define a volume; wherein the volume is a cube (cubic Bezier; col. 5, lines 42-50).

Claims 15 and 16, the rationale provided in the rejection of claim 1 is incorporated herein.

Claim 8, Loop does not teach hybrid mesh; however, Assa et al. discloses the base mesh and higher level meshes (hybrid mesh) have a hierarchical relationship (col. 11, lines 55-62; col. 12, lines 56-58; col. 13, lines 64-66). It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the hybrid mesh as taught by Assa into the method of generating smooth low degree polynomial spline surfaces over irregular meshes of Loop's teaching for producing the hybrid mesh, because it would provide multilevel resolution in a hierarchical surface (abstract).

Claim 22, Assa et al. discloses a data structure corresponding to a root polygon in a mesh (the original tree or node front of the tree; col. 2, line 41, or ancestor), polygon having vertices (col. 2, lines 61-67), neighboring polygons (col. 2, lines 55-57; col. 10, line 6), child polygons (leaf or child; col. 13, lines 50-52). a pointer to the vertices of the root polygon; a pointer to the neighboring polygons; a pointer to any child polygons (parent pointers in the quadtree nodes; col. 17, lines 63-64; col. 18, line 31). Assa teaches the parent pointers to the root and children polygons and does not teach a pointer to the neighboring polygons; however Ass teaches the mesh representation stored at the quadtree having the root (parent) and four children; therefore a pointer to the neighbors could be a pointer to any child in the data structure. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the data structure of Assa's teaching for using a pointer in the tree data

structure, because it would provide efficient retrieval of the parent nodes (col. 17, lines 62-65).

Claims 23-31, the rationale provided in the rejection of claims 5-8, 21 and 22 is incorporated herein.

Claims 32-36, the rationale provided in the rejection of claims 20-22 is incorporated herein. In addition, Assa teaches a child polygon (branch or leaf node; col. 12, lines 35-36) having a vertices, a parent (ancestor; col. 13, line 15) polygon (col. 2, lines 64-67). The child polygon is a part of a hybrid mesh (col. 12, lines 27-39); a flag indicating the child has been removed from the mesh (col. 13, lines 46-52).

Claims 37-42, the rationale provide in the rejection of claims 10, 20, 21, 28, 29, 32, 33 and 36 is incorporated herein.

5. Claims 13, 14 and 17-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Loop (5,602,979) in view of Assa et al. (6,313,837) and further in view of Krishnamurthy (6,256,038).

Claims 13 and 14, Loop does not teach parameterizing meshes; however, Krishnamurthy teaches parameterizing meshes (col. 2, lines 46-62) and performing irregular operation (approximated operation or fitting operation) after the parameterization step (col. 2, line 63 through col. 3, line 33). **Claim 17**, the rationale provided in the rejection of claims 1 and 8 is incorporated herein. In addition, Krishnamurthy teaches a base mesh comprising patches (col. 2, lines 42-44); at least one of the higher level meshes representing a patch being an irregular mesh (fitting to the patch or irregular mesh or polygonal mesh; col. 2, lines 63-67; col. 3, lines 1-52). It

would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate parameterization of the patch as taught by Krishnamurthy into the method of generating smooth low degree polynomial spline surfaces over irregular meshes of Loop's teaching for producing the hybrid mesh, because the parameterization is preferably performed such that the discretized higher order energy functional is minimized subject to the constraint that is iso-curves of the parameterization are attracted to follow a user-defined feature curve on the surface (col. 2, lines 58-62).

Claims 18 and 19, the rationale provided in the rejection of claims 2 and 3 is incorporated herein.

Claims 20 and 21, Loop teaches a processor readable medium, a memory (col. 7, line 65 through col. 8, line 21).

6. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Loop (5,602,979) in view of Assa et al. (6,313,837) and further in view of Gueziec et al. (6,184,897).

Claims 9 and 10, Loop does not teach cutting a hole in a mesh; however, Gueziec et al. discloses irregular operation comprises cutting a hole in a mesh (cu operation; col. 10, lines 8-15) by removing polygons (col. 10, lines 33-34); adding one or more polygons to a mesh (fig. 13, # 13300). It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the cutting, removing and adding operations as taught by Gueziec into the method of generating smooth low degree polynomial spline surfaces over irregular meshes of Loop's teaching

for producing the hybrid mesh, because it would provide multi-resolution of level of detail (col. 3, lines 49-55).

Allowable Subject Matter

7. Claims 43-48 allowed.

The following is an examiner's statement of reasons for allowance:

Claims 43-48, the closest prior art Guskov et al. "Normal Meshes" (ACM 2000 discloses applying a wavelet transform to transform the hybrid mesh into wavelet coefficients (page 97, the right column, lines 1-14). Guskov does not teach encoding the wavelet coefficients with a progressive encoding algorithm; applying a progressive decoding algorithm to the coded mesh to recover wavelet coefficients

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

8. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

With respect to applicant's arguments, the rejection of claims 1-42 has been modified in this Office Action. Loop teaches forming a base mesh (input mesh M0; col. 6, lines 5-6); forming one or more higher level meshes (new meshes M1 and M2; col. 6,

lines 8-11) from the base mesh through regular refinement operations in combination with irregular operation (isolating irregularities and constraining geometry or constrained refinement operation; col. 6, lines 5-7); Loop does not teach the hybrid mesh representation comprising the base mesh in combination with one or more higher level meshes; however, Assa et al. teaches a hierarchical surface representation is an architecture of a hybrid-grid mesh (col. 11, lines 54-67), because the quadtree hierarchy provides a multiresolution hierarchy which has an ancestor (coarsest level of base mesh) and four children (higher levels), the hybrid grid-mesh representation supports general topological and geometrical editing, the hybrid architecture maintains the flexibility to provide the irregular refinement of a grid (col. 12, lines 1-52). Both Loop and Assa teach irregular operations: isolating irregularities and constraining geometry or constrained refinement operation; Loop's reference, col. 6, lines 5-7; Assa's reference, col. 9, line 66 through col. 10, line 16).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Kimbinh Nguyen** whose telephone number is **(703) 305-9683**. The examiner can normally be reached **(Monday- Thursday from 7:00 AM to 4:30 PM and alternate Fridays from 7:00 AM to 3:30 PM)**.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Zimmerman, can be reached at (703) 305-9798.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Part II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

April 23, 2004

Kimbinh Nguyen

Patent Examiner AU 2671